MP0798 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. ______________

Application No.:	10/686,151
Filing Date:	October 15, 2003
Appellant:	Dinesh Jayabharathi et al.
Conf. No.:	
Group Art Unit:	2138
Examiner:	Dipakkumar B. Gandhi
Title:	SYSTEM AND METHOD FOR USING TAP CONTROLLERS

BRIEF ON APPEAL ON BEHALF OF APPELLANTS AND PETITION FOR EXTENSION OF TIME

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November 13, 2007

Sir:

This appeal is from the decision of the Patent Examiner dated April 26, 2007, rejecting claims 1-35, which are reproduced in Appendix A of this Appeal Brief.

Appellant hereby petitions under the provisions of 37 C.F.R. § 1.136(a) for an extension of time in which to respond to the outstanding Office Action and includes a fee as set forth in 37 C.F.R. § 1.17(a) with this response for such extension of time.

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1. (Previously Presented) A method for dynamically writing to an internal register space of a chip using a test access port ("TAP") controller without interfering with normal operation of the chip, comprising: 12
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BRIEF ON APPEAL ON BEHALF OF APPELLANT

In support of the Notice of Appeal filed July 26, 2007, appealing the Examiner's Rejection of each of claims 1-35, mailed April 26, 2007, which appear in the attached Appendix A, Appellant hereby provides the following remarks.

I. REAL PARTY IN INTEREST

The present application is assigned to Marvell International, Ltd. as recorded in the Patent and Trademark Office at Reel 014668, Frame 0234 and Reel 017017, Frame 0450.

II. RELATED APPEALS AND INTERFERENCES

The undersigned, the Assignee, and the Appellant do not know of any other appeals or interferences which would directly affect or that would be directly affected by, or have a bearing on, the Board's decision in this Appeal.

III. STATUS OF THE CLAIMS

Claims 1-35 are reproduced in the attached Appendix A and are the claims on Appeal. Each of these claims is currently pending in the application.

IV. STATUS OF THE AMENDMENTS

There are no pending amendments filed subsequent to a final rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Storage controllers (such as hard disk drive controllers) may include one or more integrated circuits (ICs). Internal register files of ICs store data during operation of the ICs. This data may be accessed during testing of the ICs.

After assembly within a storage controller (e.g. arrangement on an internal printed circuit board), ICs may be tested according to a standard such as a Joint Task Action Group (JTAG) standard. The JTAG standard allows testing of ICs internal to a storage controller via a test access port (TAP). A TAP controller may be used to access internal data (i.e. data stored in internal registers) of ICs via the TAP. Conventionally, all IC operations are halted when the internal data is accessed via the TAP.

As described in Paragraph [0032] on Page 8 of the present application, a TAP controller 119 allows access to internal registers of a system 100A without interfering with normal operation of the system 100A (i.e. without halting normal operation). Independent claim 1 recites a method for dynamically writing to an internal register space (e.g. internal register space 121, see FIG. 1B and Page 9, Lines 1-5) of a chip using a TAP controller (e.g. TAP controller interface 119, see FIG. 1B and Page 10, Lines 1-5) without interfering with normal operation of the chip. The method includes loading write instructions and addresses of the internal register space where data is to be written (e.g. instructions and addresses corresponding to the internal register space 121 are loaded into register 210, see FIG. 2 and Page 10, Lines 20-22). Access is gained through arbitration to the internal register space during normal operation of the chip (see FIGS. 3 and 4 and Page 12, Lines 12-21).

Independent claim 4 recites similar subject matter, including gaining access to the internal register space 121 during normal operation of the chip, and transferring information to a register in the TAP controller 119 (e.g. data is transferred to data register 210 of the TAP controller 119, see FIG. 3 and Page 11, Lines 24-26). Independent claim 7 recites similar subject matter, including an arbitration module (e.g. arbiter 122, see FIG. 1B and Page 9, Lines 6-11). Independent claim 12 recites similar subject matter, including a data register (e.g. internal data register 210, see FIG. 2 and

Page 10, Lines 1-5) where data is stored after the TAP controller 119 reads it from the internal register space 121, and/or where data that is to be written into the internal register is first written to the data register.

Independent claim 14 recites a method for accessing internal memory of a disk controller (e.g. controller 101, see FIG. 1A and Page 7, Lines 9-10), comprising storing disk controller control data on a first memory that is located on the disk controller (e.g. internal register space 121, see FIG. 1B and Page 9, Lines 1-5), requesting the control data from the first memory (see Page 9, Lines 6-11), and transferring the control data form the first memory to a second memory (e.g. registers 208 and 210, see FIG. 2 and Page 11, Lines 24-26), wherein the second memory is located on a TAP controller (see FIG. 2; e.g. registers 208 and 210 are located on the TAP controller 119) and the TAP controller is located on the disk controller (see FIG. 1A; e.g. the TAP controller 119 is located on the controller 101).

Independent claim 22 recites similar subject matter, including a first memory that stores disk controller data (e.g. internal register space 121, see FIG. 1B and Page 9, Lines 1-5), a TAP controller 119 that communicates with the first memory, and a second memory that is located on the TAP controller 119 (e.g. registers 208 and 210, see FIG. 2 and Page 11, Lines 24-26), wherein the TAP controller 119 receives a request for the control data from a device that is external to the disk controller (e.g. TAP controller port 120, see FIGS. 1A and 1B) and transfers the control data form the first memory to the second memory.

Independent claim 29 recites similar subject matter, including first memory means for storing disk controller data (e.g. internal register space 121, see FIG. 1B and Page 9, Lines 1-5), TAP controller means (e.g. TAP controller 119) for communicating with the first memory means, and second memory means that is located on the TAP controller means (e.g. registers 208 and 210, see FIG. 2 and Page 11, Lines 24-26), wherein the TAP controller means receives a request for the control data from a device that is external to the disk controller (e.g. TAP controller port 120, see FIGS. 1A and 1B) and transfers the control data form the first memory means to the second memory means.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant seeks the Board's review of the rejection of:

(a) Claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over Henson et al. (European Pat. No. 0622726 A2, hereinafter "Henson") in view of Szczepanek et al. (U.S. Pub. No. 2003/0110344, hereinafter "Szczepanek").

(b) Claims 14-35 under 35 U.S.C. § 103(a) as being unpatentable over Henson in view of Szczepanek and Noguchi (U.S. Pub. No. 2002/00626466 A1, hereinafter "Noguchi").

VII. ARGUMENTS

A. The Rejections

The rejections that are the subject of this appeal are: a rejection of each of independent claims 1, 4, 7, and 12 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Henson in view of Szczepanek, and a rejection of each of independent claims 14, 22, and 29 under 35 U.S.C. § 103(a) as allegedly being unpatentable Henson in view of Szczepanek and Noguchi.

With respect to independent claims 1, 4, and 7, the Examiner alleges that Szczepanek teaches that "during normal operation, internal RAM access can be effected using the DIO interface." (See Page 2, Lines 19-20 of the Office Action mailed April 26, 2007, hereinafter "the Final Office Action"). The Examiner further alleges that Henson teaches "the buffer controller circuit including an access arbitration circuit for arbitrating requests for access to the cache buffer." (See Page 2, Lines 22-24 of the Final Office Action).

With respect to independent claim 12, the Examiner alleges that Henson teaches that "during reading operations, the microprocessor would load a starting address into the address register, and then wait for the delay time needed by the memory controller in fetching the byte from the cache buffer memory array into the data register. (See Page 3, Lines 6-9 of the Final Office Action).

With respect to independent claim 14, the Examiner alleges that Henson teaches that "the second memory is located on a TAP controller. (See Page 3, Lines 21-22 of the Final Office Action). The Examiner rejects independent claims 22 and 29 for similar reasons.

B. Claim Distinctions

1. Distinctions regarding independent Claims 1, 4, and 7

Appellant respectfully submits that the alleged combination fails to disclose a method for dynamically writing to an internal register space of a chip using a TAP controller without interfering with normal operation of the chip. In particular, claim 1 recites writing to the internal register space **without interfering with normal operation of the chip**. Further, claim 1 recites the step of gaining access through arbitration to the internal register space **during normal operation of the chip**.

As best understood by Appellant, the alleged combination fails to disclose this limitation. For example, the Examiner relies on Szczepanek to disclose "indirect access to internal registers and SRAM." (See Page 3, Lines 1-3 of the Office Action mailed October 13, 2006, hereinafter "the Office Action"). Appellant respectfully submits that Szczepanek fails to disclose reading from and/or writing to internal register space using a TAP controller **during normal chip operation**. Instead, Szczepanek discloses accessing RAM **during testing**. For example, Paragraph [0416] of Szczepanek recites:

> Parallel Module Test **uses the JTAG TAP controller during testing** to control test access to the embedded RAM blocks directly from the external pins. (Emphasis added).

In other words, this cited portion clearly states that the TAP controller accesses the chip during testing, not during normal chip operation. As described in Appellant's specification, typically **all normal chip operations stop during JTAG testing, thereby interfering with normal operation of the chip**. (See Paragraph [0008] of the present application). Szczepanek appears to be absent of any teaching or suggestion of allowing access to internal register space during normal chip operation as claim 1 recites and instead discloses allowing the TAP controller access during testing, which directly contradicts the limitations of claim 1.

The Examiner fails to address this cited portion of Szczepanek. Further, Appellant respectfully notes that claim 1 recites gaining access to **internal register space of a chip**. In contrast, the above cited portion relates to internal RAM access. Appellant notes that internal register space of a chip, such as an IC, is not equivalent to RAM. As such, neither the above cited portion nor any other portion of Szczepanek discloses **gaining access to internal register space during normal operation of the chip**.

Appellant respectfully submits that Szczepanek, either singly or in combination with Henson, fails to disclose providing access to i) internal register space of a chip ii) during normal operation of the chip. As such, claim 1 should be allowable for at least the above reasons. Claims 4 and 7 should be allowable for at least similar reasons.

2. Dependent Claims 2-3, 5-6, and 8-11

With regard to claims 2-3, 5-6, and 8-11 these claims are allowable for at least the reasons previously presented with regard to claims 1, 4, and 7, respectively. Accordingly, it is respectfully requested that the rejection of these claims be overturned.

3. Distinctions regarding independent Claims 12, 14, 22, 29

Appellant respectfully submits that the alleged combination of Henson, Szczepanek, Henson, and Noguchi fails to disclose transferring **disk controller control data** from a first memory on a disk controller **to a second memory located on a TAP controller**, where the TAP controller is also located on the disk controller. Instead, the combination appears to disclose transferring **JTAG test instructions, not disk controller control data**, to the alleged second memory, and fails to disclose that the second memory is located on the TAP controller.

For example, the Examiner initially alleged that Szczepanek discloses this limitation at Page 29, Paragraphs [0408]-[0416]. Applicant respectfully disagrees. Instead, the cited portions of Szczepanek appear to disclose **transferring JTAG instructions**. More specifically, Table 9 (see Paragraph [0411]) illustrates JTAG opcodes, including EXTEST, SAMPLE/PRELOAD, ATPG, SELF EXERCISE, IDCODE, HIGHZ, and BYPASS, for example. **This alleged data is not disk controller control data as claim 14 recites**. As such, Szczepanek fails to disclose transferring anything other than JTAG instructions to the alleged second memory.

The Examiner now alleges that Henson discloses this limitation at Column 3, Lines 17-22. This cited portion of Henson recites "during reading operations, the microprocessor would load a starting address into the address register, and then wait for the delay time needed by the memory controller in fetching the byte from the cache buffer memory array into data register." Appellant respectfully notes that this cited portion still fails to make up for the deficiency of Szczepanek. In particular, this cited portion fails to disclose transferring control data to **a second memory located on a TAP controller**. As such, neither Szczepanek nor Henson discloses transferring control data from a first memory located on the disk controller to a second memory located on a TAP controller.

Further, claim 14 recites that the disk controller control data is transferred **from a first memory located on the disk controller to a second memory located on the TAP controller**. The alleged data of Szczepanek **is not transferred from a first memory located on a disk controller to a second memory located on the TAP controller**. As best understood by Appellant, this alleged data, being JTAG instructions, is inherently stored on the alleged TAP controller, or is transferred from an external location (e.g. via a TAP port) to the TAP controller.

Appellant further notes that Henson fails to make up for the deficiencies of Szczepanek because **Henson is absent of any teaching or suggestion of a TAP controller**. Initially, the Examiner **acknowledged that Henson does not disclose a TAP controller**. (See Page 2 of the Office Action mailed April 7, 2006). In direct contradiction to this acknowledgment and the disclosure of Henson, the Examiner now states that "Henson teaches that the second memory is located on a test access port controller," citing FIG. 1 of Henson. (See Page 3, Lines 21-22 of the Final Office Action). Here again, Appellant respectfully submits that neither FIG. 1 nor any other figure of Henson appears to make any mention of a TAP controller. As such, Appellant fails to comprehend how Henson can disclose that the claimed second memory is located on the TAP controller when Henson is absent of any teaching or suggestion of the TAP controller.

Appellant respectfully submits that Henson, either singly or in combination with the other cited prior art references, fails to disclose a TAP controller located on a disk controller, a second memory located on the TAP controller, and transferring control data from a first memory located on the disk controller to the second memory. Accordingly, Appellant respectfully submits that claim 14 should be allowable for at least the above reasons. Claims 12, 22, and 29 should be allowable for at least similar reasons.

4. Dependent Claims 13, 15-21, 23-28, and 30-35

With regard to claims 13, 15-21, 23-28, and 30-35 these claims are allowable for at least the reasons previously presented with regard to claims 12, 14, 22, and 29, respectively. Accordingly, it is respectfully requested that the rejection of these claims be overturned.

VIII. CONCLUSION

Appellant respectfully request the Honorable Board of Patent Appeals and Interferences to reverse the Examiner's rejection of each of pending claims 1-35. Appellant respectfully submits that the prior art does not teach or suggest one or more limitations of the claims as discussed above. Accordingly, for at least the aforementioned reasons, Appellant respectfully requests the Honorable members of the Board of Patent Appeals and Interferences to reverse the outstanding rejections in connection with the present application and permit each of claims 1-35 to be passed to allowance in connection with the present application.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Damian M. Aquino, Reg. No. 54,964, at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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IX. APPENDIX A

CLAIMS APPENDED

This is a complete and current listing of the claims.

1. (Previously Presented) A method for dynamically writing to an internal register space of a chip using a test access port ("TAP") controller without interfering with normal operation of the chip, comprising:

loading write instructions and address of the internal register space where data is to be written; and

gaining access through arbitration to the internal register space during normal operation of the chip.

2. (Original) The method of Claim 1, wherein data that is to be written is loaded into a register in the TAP controller before being written in the internal register space.

3. (Original) The method of Claim 1, wherein the write instructions are loaded into an instruction register of the TAP controller.

4. (Previously Presented) A method for dynamically reading from an internal register space of a chip using a test access port ("TAP") controller without interfering with normal operation of the chip, comprising:

loading a read command in an instruction register;

loading an address of the internal register space from where data is to be read, to a data register;

gaining access to the internal register space during normal operation of the chip; and

transferring information to a register in the TAP controller.

5. (Original) The method of Claim 4, wherein access to the internal register space is gained using an arbitration module.

6. (Original) The method of Claim 4, wherein the instruction register is located in the TAP controller.

7. (Previously Presented) A system of accessing an internal register space of a chip using a test access port ("TAP") controller without interfering with normal operation of the chip, comprising:

an instruction register in the TAP controller to which read and/or write instructions are written; and

an arbitration module that receives an input from the TAP controller when the TAP controller needs to access the internal register space during normal operation of the chip.

8. (Original) The system of Claim 7, wherein write instructions are loaded in the instruction register and address of the internal register space where data is to be written is loaded into a data register.

9. (Original) The system of Claim 7, wherein an address of the internal register space from where data is to be read is loaded to the data register.

10. (Original) The system of Claim 7, wherein after the TAP controller reads data from the internal register space it is stored in the data register.

11. (Original) The system of Claim 10, wherein data that is to be written into the internal register space is first written to the data register.

12. (Previously Presented) A test access port ("TAP") controller for dynamically accessing an internal register space in a chip without interfering with normal operation of the chip, comprising:

an instruction register in the TAP controller to which read and/or write instructions are written; and

a data register where data is stored after the TAP controller reads it from the internal register space, and/or where data that is to be written into the internal register is first written to the data register.

13. (Original) The TAP controller of Claim 12, wherein before accessing the internal register space, the TAP controller requests access to an arbitration module.

14. (Previously Presented) A method for accessing internal memory of a disk controller, comprising:

storing disk controller control data on a first memory that is located on the disk controller;

requesting the control data from the first memory; and

transferring the control data from the first memory to a second memory, wherein the second memory is located on a test access port controller and the test access port controller is located on the disk controller.

15. (Previously Presented) The method of claim 14 further comprising transferring the control data from the second memory to a device that is external to the disk controller.

16. (Previously Presented) The method of claim 14 further comprising loading at least one of a write instruction, a read instruction, and a memory address that corresponds to the first memory into the second memory.

17. (Previously Presented) The method of claim 14 further comprising providing access to the first memory with an arbitration module.

18. (Previously Presented) The method of claim 14 wherein at least one of the first memory and the second memory is a register.

19. (Previously Presented) The method of claim 14 further comprising:
writing data to the first memory; and
subsequently writing the data to the second memory.

20. (Previously Presented) The method of claim 14 further comprising:
loading a read command in the second memory;
loading an address of the first memory in the second memory;
transferring the control data from the first memory to the second memory according to the read command and the address.

21. (Previously Presented) The method of claim 14, further comprising acquiring access to the second memory using an arbitration module.

22. (Previously Presented) A disk controller comprising:
a first memory that stores disk controller control data;
a test access port controller that communicates with the first memory; and
a second memory that is located on the test access port controller,
wherein the test access port controller receives a request for the control data from a device that is external to the disk controller and transfers the control data from the first memory to the second memory.

23. (Previously Presented) The disk controller of claim 22 wherein the test access port controller transfers the control data from the second memory to the device.

24. (Previously Presented) The disk controller of claim 22 wherein the test access port controller loads at least one of a write instruction, a read instruction, and a memory address that corresponds to the first memory into the second memory.

25. (Previously Presented) The disk controller of claim 22 further comprising an arbitration module that receives a request from the test access port controller to access the first memory.

26. (Previously Presented) The disk controller of claim 22 wherein at least one of the first memory and the second memory is a register.

27. (Previously Presented) The disk controller of claim 22 wherein the test access port controller writes data to the first memory and subsequently writes the data to the second memory.

28. (Previously Presented) The disk controller of claim 22 wherein the test access port controller loads a read command in the second memory, loads an address of the first memory in the second memory, and transfers the control data from the first memory to the second memory according to the read command and the address.

29. (Previously Presented) A disk controller comprising:

first memory means for storing disk controller control data;

test access port controller means for communicating with the first memory; and

second memory means that is located on the test access port controller means,

wherein the test access port controller means receives a request for the control data from a device that is external to the disk controller and transfers the control data from the first memory means to the second memory means.

30. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means transfers the control data from the second memory means to the device.

31. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means loads at least one of a write instruction, a read instruction, and a memory address that corresponds to the first memory means into the second memory means.

32. (Previously Presented) The disk controller of claim 29 further comprising arbitration means for receiving a request from the test access port controller means to access the first memory means.

33. (Previously Presented) The disk controller of claim 29 wherein at least one of the first memory means and the second memory means is a register.

34. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means writes data to the first memory means and subsequently writes the data to the second memory means.

35. (Previously Presented) The disk controller of claim 29 wherein the test access port controller means loads a read command in the second memory means, loads an address of the first memory means in the second memory means, and transfers the control data from the first memory means to the second memory means according to the read command and the address.

X. APPENDIX B

EVIDENCE APPENDED

A copy of the Office Action mailed April 26, 2007 is attached.

XI. APPENDIX C

RELATED PROCEEDINGS APPENDED

There are no related proceedings.